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<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> (21) Internationales Aktenzeichen: PCT/DE98/00334 (22) Internationales Anmeldedatum: 7. Februar 1998 (07.02.98) (30) Prioritätsdaten: 197 04 728.9 8. Februar 1997 (08.02.97) DE (71) Anmelder (für alle Bestimmungsstaaten ausser US): PACT INFORMATIONSTECHNOLOGIE GMBH [DE/DE]; Thelemannstrasse 15, D-81545 München (DE). (72) Erfinder; und (75) Erfinder/Anmelder (nur für US): VORBACH, Martin [DE/DE]; (DE). MÜNCH, Robert [DE/DE]; Hagebuttenweg 36, D-76149 Karlsruhe (DE). (74) Anwalt: ZAHN, Roland; Im Speitel 102, D-76229 Karlsruhe (DE). </div> <div style="width: 50%;"> (81) Bestimmungsstaaten: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO Patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), eurasisches Patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), europäisches Patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI Patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Veröffentlicht <i>Ohne internationalen Recherchenbericht und erneut zu veröffentlichen nach Erhalt des Berichts.</i> </div> </div>		

(54) Title: METHOD FOR SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE COMPONENT

(54) Bezeichnung: VERFAHREN ZUR SELBSTSYNCHRONISATION VON KONFIGURIERBAREN ELEMENTEN EINES PROGRAMMIERBAREN BAUSTEINES

(57) Abstract

The invention relates to a method for synchronization and reconfiguration of configurable elements in components with two-dimensional or multidimensional programmable cell structure (DFP, FPGA, DPGA, RAW machine) as well as to the control of conditioned branches in common microprocessors, digital signal processors and microcontrollers. According to said method, synchronization signals are generated during processing within the data flow by the elements that are to be processed and configured by means of comparisons, algebraic signs, transmission of arithmetic operations, error status or the like, and are sent to additional elements for synchronization via the data bus.

Configuration words within a configurable element are generated from the data flow on the basis of corresponding commands and communicated, along with the address of the register to be picked up, to a further configurable element via the data bus, wherein said element is thus (re)configured without the influence of an external load logic. A valid configuration of the configurable elements from a plurality of configurations or a valid command from multiple possible commands of an arithmetic processing unit is then selected during running time on the basis of synchronization signals.

